
dsPIC30F4011/4012 Rev. A2 Silicon Errata

dsPIC30F4011/4012 (Rev. A2) Silicon Errata

The dsPIC30F4011/4012 (Rev. A2) samples you have received were found to conform to the specifications and functionality described in the following documents:

- DS70030 – dsPIC30F Programmer’s Reference Manual
- DS70135 – dsPIC30F4011, dsPIC30F4012 Data Sheet
- DS70046 – dsPIC30F Family Reference Manual

The exceptions to the specifications in the documents listed above are described in this section. The specific devices for which these exceptions are described are listed below:

- dsPIC30F4011
- dsPIC30F4012

These devices may be identified by the following message that appears in the MPLAB® ICD 2 Output Window under MPLAB IDE, when a “reset-and-connect” operation is performed within MPLAB IDE:

```
Setting Vdd source to target
Target Device dsPIC30F4012 found,
revision = Rev 0x1002
...Reading ICD Product ID
Running ICD Self Test
...Passed
MPLAB ICD 2 Ready
```

The errata described in this section will be fixed in future revisions of dsPIC30F4011 and dsPIC30F4012 devices.

Silicon Errata Summary

The following list summarizes the errata described in further detail throughout the remainder of this document:

1. **Decimal Adjust Instruction**
The Decimal Adjust instruction, `DAW.b`, may improperly clear the Carry bit, `C (SR<0>)`.
2. **Special Function Registers**
Writes to certain unimplemented address locations can affect I/O Port register values.
3. **PSV Operations Using SR**
In certain instructions, fetching one of the operands from program memory using Program Space Visibility (PSV) will corrupt specific bits in the Status Register, SR.
4. **Early Termination of Nested DO Loops**
When using two DO loops in a nested fashion, terminating the inner-level DO loop by setting the EDT (`CORCON<11>`) bit will produce unexpected results.
5. **x4 PLL Operation**
The x4 PLL mode of operation may not function correctly for certain input frequencies.
6. **Sequential Interrupts**
Sequential interrupts after modifying the CPU IPL, interrupt IPL, interrupt enable or interrupt flag may cause an Address Error trap.
7. **Using OSC2/RC15 pin for Digital I/O**
For this revision of silicon, if the pin RC15 is required for digital input/output, the `FPR<4:0>` bits in the FOSC Configuration register may not be set up for FRC w/PLL 4x/8x/16x modes.

The following sections will describe the errata and work around to these errata, where they may apply.

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1. Module: CPU – DAW.b Instruction

The Decimal Adjust instruction, DAW.b, may improperly clear the Carry bit, C (SR<0>), when executed.

Work around

Check the state of the Carry bit prior to executing the DAW.b instruction. If the Carry bit is set, set the Carry bit again after executing the DAW.b instruction. Example 1 shows how the application should process the Carry bit during a BCD addition operation.

EXAMPLE 1:

```
.include "p30f4012.inc"
.....
MOV.b  #0x80, w0  ;First BCD number
MOV.b  #0x80, w1  ;Second BCD number
ADD.b  w0, w1, w2 ;Perform addition
BRA    NC, L0     ;If C set go to L0
DAW.b  w2         ;If not,do DAW and
BSET.b SR, #C    ;set the carry bit
BRA    L1         ;and exit
L0:DAW.b  w2
L1: .....
```

2. Module: Special Function Registers

The I/O Port register values can be changed by writing to the following address locations, which are located in unimplemented memory space. A write to these unimplemented addresses could cause an I/O pin configured as an output to change states. This state change could be confirmed by reading either the Port or LAT register associated with the pin.

PORTB will be modified by a write to address 0x0C8
PORTC will be modified by a write to address 0x0CE
PORTD will be modified by a write to address 0x0D4
PORTE will be modified by a write to address 0x0DA
PORTF will be modified by a write to address 0x0E0

Work around

User software should avoid writing to the unimplemented locations listed above.

3. Module: PSV Operations Using SR

When one of the operands of instructions shown in Table 1 is fetched from program memory using Program Space Visibility (PSV), the Status Register, SR and/or the results may be corrupted. These instructions are identified in Table 1. Example 2 demonstrates one scenario where this occurs.

TABLE 1:

Instruction ⁽²⁾	Examples of Incorrect Operation	Data Corruption IN
ADDC	ADDC W0, [W1++], W2 ;See Note 1	SR<1:0> bits ⁽³⁾ , Result in W2
SUBB	SUBB.b W0, [++W1], W3 ;See Note 1	SR<1:0> bits ⁽³⁾ , Result in W3
CPB	CPB W0, [W1++], W4 ;See Note 1	SR<1:0> bits ⁽³⁾
RLC	RLC [W1], W4 ;See Note 1	SR<1:0> bits ⁽³⁾ , Result in W4
RRC	RRC [W1], W2 ;See Note 1	SR<1:0> bits ⁽³⁾ , Result in W2
ADD (Accumulator-based)	ADD [W1++], A ;See Note 1	SR<1:0> bits ⁽⁴⁾
LAC	LAC [W1], A ;See Note 1	SR<15:10> bits ⁽⁴⁾

- Note 1:** The errata only affects these instructions when a PSV access is performed to fetch one of the source operands in the instruction. A PSV access is performed when the Effective Address of the source operand is greater than 0x8000 and the PSV (CORCON<2>) bit is set to '1'. In the examples shown, the data access from program memory is made via the W1 register.
- 2:** Refer to the Programmer's Reference Manual for details on the dsPIC30F instruction set.
- 3:** SR<1:0> bits represent Sticky Zero and Carry status bits respectively.
- 4:** SR<15:10> bits represent Accumulator Overflow and Saturation status bits

EXAMPLE 2:

```
.include "p30fxxxx.inc"
.....
MOV.B #0x00, W0      ;Load PSVPAG register
MOV.B WREG, PSVPAG
BSET CORCON, #PSV   ;Enable PSV
....
MOV #0x8200, W1     ;Set up W1 for
                   ;indirect PSV access
                   ;from 0x000200
ADD W3, [W1++], W5 ;This instruction
                   ;works ok
ADDC W4, [W1++], W6 ;Carry flag and
                   ;W6 gets
                   ;corrupted here!
```

Work around

Work Around 1: For Assembly Language Source Code

To work around the erratum in the MPLAB[®] ASM30 assembler, the application may perform a PSV access to move the source operand from program memory to RAM or a W register prior to performing the operations listed in Table 1. The work around for Example 2 is demonstrated in Example 3.

EXAMPLE 3:

```
.include "p30fxxxx.inc"
.....
MOV.B #0x00, w0     ;Load PSVPAG register
MOV.B WREG, PSVPAG
BSET CORCON, #PSV  ;Enable PSV
....
MOV #0x8200, W1     ;Set up W1 for
                   ;indirect PSV access
                   ;from 0x000200
ADD W3, [W1++], W5 ;This instruction
                   ;works ok
MOV [W1++], W2     ;Load W2 with data
                   ;from program memory
ADDC W4, W2, W6    ;Carry flag and W4
                   ;results are ok!
```

Work Around 2: For C Language Source Code

For applications using C language, MPLAB C30 versions 1.20.04 or higher provide the following command-line switch that implements a work around for the erratum.

```
-merrata=psv
```

Refer to the "readme.txt" file in the MPLAB C30 v1.20.04 toolsuite for further details.

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4. Module: Early Termination of Nested DO Loops

When using two DO loops in a nested fashion, terminating the inner-level DO loop by setting the EDT (CORCON<11>) bit will produce unexpected results. Specifically, the device may continue executing code within the outer DO loop forever. This erratum does not affect the operation of the MPLAB C30 compiler.

Work around

The application should save the DCOUNT SFR prior to entering the inner DO loop and restore it upon exiting the inner DO loop. This work around is shown in Example 4.

EXAMPLE 4:

```
.include "p30fxxxx.inc"
.....
DO #CNT1, LOOP0      ;Outer loop start
....
PUSH DCOUNT        ;Save DCOUNT
DO #CNT2, LOOP1     ;Inner loop
....               ;starts
BTSS Flag, #0
BSET CORCON, #EDT  ;Terminate inner
....               ;DO-loop early
....
LOOP1: MOV W1, W5    ;Inner loop ends
POP DCOUNT         ;Restore DCOUNT
...
LOOP0: MOV W5, W8    ;Outer loop ends
```

Note: For details on the functionality of EDT bit, see section 2.9.2.4 in the dsPIC30F Family Reference Manual.

5. Module: PLL

When the x4 PLL mode of operation is selected, the specified input frequency range of 4-10 MHz is not fully supported.

When device VDD is 2.5-3.0V, the x4 PLL input frequency must be in the range of 4-5 MHz. When device VDD is 3.0-3.6V, the x4 PLL input frequency must be in the range of 4-6 MHz for both industrial and extended temperature ranges.

Work around

1. Use x8 PLL or x16 PLL mode of operation and set final device clock speed using the POST<1:0> oscillator postscaler control bits (OSCCON<7:6>).
2. Use the EC without PLL Clock mode with a suitable clock frequency to obtain the equivalent x4 PLL clock rate.

6. Module: Interrupt Controller – Sequential Interrupts

When interrupt nesting is enabled (or NSTDIS (INTCON1<15>) bit is '0'), the following sequence of events will lead to an Address Error trap. The generic terms "Interrupt 1" and "Interrupt 2" are used to represent any two enabled dsPIC30F interrupts.

1. Interrupt 1 processing begins.
2. Interrupt 1 is negated by user software by one of the following methods:
 - CPU IPL is raised to Interrupt 1 IPL level or higher or
 - Interrupt 1 IPL is lowered to CPU IPL level or lower or
 - Interrupt 1 is disabled (Interrupt 1 IE bit set to '0') or
 - Interrupt 1 flag is cleared
3. Interrupt 2 with priority higher than Interrupt 1 occurs.

Work around

The user may disable interrupt nesting or execute a DISI instruction before modifying the CPU IPL or Interrupt 1 setting. A minimum DISI value of 2 is required if the DISI is executed immediately before the CPU IPL or Interrupt 1 is modified, as shown in Example 5. If the MPLAB C30 compiler is being used, one must inspect the Disassembly Listing in the MPLAB IDE file to determine the exact number of cycles to disable level 1-6 interrupts. One may use a large DISI value and then set the DISICNT register to zero, as shown in Example 6. A macro may also be used to perform this task, as shown in Example 7.

EXAMPLE 5:

```
.include      "p30fxxxx.inc"
...
DISI    #2                ; protect the disable of INT1
BCLR    IEC1, #INT1IE    ; disable interrupt 1
...                ; next instruction protected by DISI
```

EXAMPLE 6:

```
.include      "p30fxxxx.h"
...
__asm__ volatile ("DISI #0x1FFF"); // protect CPU IPL modification
SRbits.IPL = 0x5;                // set CPU IPL to 5
DISICNT = 0x0;                   // remove DISI protection
```

EXAMPLE 7:

```
#define DISI_PROTECT(X) {          \
    __asm__ volatile ("DISI #0x1FFF"); \
    X;                               \
    DISICNT = 0; }

DISI_PROTECT(SRbits.IPL = 0x5); // safely modify the CPU IPL
```

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7. Module: Using OSC2/RC15 pin for Digital I/O

The port pin, RC15, is multiplexed with the primary oscillator pin, OSC2. When pin RC15 is required for digital input/output, specific bits in the Oscillator Configuration register, FOSC, may be set up as follows:

- FOS<2:0> (FOSC<10:8>) bits configured for LP, LPRC, FRC, ECIO, ERCIO or ECIO w/PLL 4x/8x/16x
- FPR<4:0> (FOSC<4:0>) bits may be configured for ECIO w/PLL 4x/8x/16x

For this revision of silicon, if the RC15 digital I/O port function is desired, the FPR<4:0> bits in the FOSC Configuration register may not be set up for FRC w/PLL 4x/8x/16x modes.

Work around

None. In future revisions of silicon, port pin RC15 may also be configured for digital I/O when the FPR<4:0> bits in the FOSC Configuration register are set up for FRC w/PLL 4x/8x/16x modes.

APPENDIX A: REVISION HISTORY

Revision A (10/2004)

Original version of the document.

Revision B (11/2004)

Added silicon issues 3 (PSV Operations Using SR) and 4 (Early Termination of Nested DO Loops).

Revision C (3/2005)

Added silicon issues 5 (PLL) and 6 (Interrupt Controller – Sequential Interrupts).

Revision D (4/2005)

Added silicon issue 7 (Using OSC2/RC15 pin for Digital I/O).

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